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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,595	03/30/2004	Andrej Zdravkovic	ATI-000148BT.1	4389

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EXAMINER	
DOGAN, ERIN L	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,595	ZDRAVKOVIC, ANDREJ	
	Examiner	Art Unit	
	Erin L. Dogan	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *45* is/are allowed.

6)☒ Claim(s) *11-28,30,32-35,38,40 and 41* is/are rejected.

7)☒ Claim(s) *29,31,36,37,39 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-45 are pending in the application.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-12, 15, 17,19-28, 30, 32-35, 38, and 40-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams (US 5,774,704).

3. For Claim 11, Williams discloses a method of reducing power consumption of a system having at least one processor, the processor being coupled to at least one queue which stores instructions for execution by the processor, the method comprising:

(a) analyzing at least one input; (b) estimating the load of the system based, at least in part, on the analysis of step (a); (c) determining a clock rate based, at least in part, on the estimation of step (b); and (d) clocking the processor at the clock rate determined in step (c) (Column 4, lines 18-22, 34-40).

4. For Claim 12, Williams discloses a method wherein the input includes at least one instruction for processing by the processor (Column 4, lines 18-22).

5. For Claim 15, Williams discloses a method wherein the at least one instruction is generated in response to a user input (Column 2, lines 12-18).

6. For Claim 17, Williams discloses a method wherein the at least one instruction is generated in response to the temperature of the processor (Column 5, lines 41-44).

7. For Claims 19 and 20, Williams discloses a method of reducing power consumption of a system having at least one processor, the method comprising:

> (a) analyzing at least one input; (b) estimating a desired processing speed based, at least in part, on the analysis of step (a); (c) determining a clock rate based on the estimation of step (b); and (d) clocking the processor at the clock rate determined in step (c) (Column 2, lines 43-51) .

8. For Claim 21, Williams discloses a method of reducing power consumption of a system having at least one processor, the processor being in communication with at least one queue which stores instructions for execution, the method comprising: controlling the clocking frequency of the processor in response to a prediction of the load of the system, the load being based, at least in part, on the instructions stored in the queue(Column 4, lines 18-22, 34-40).

9. For Claim 22, Williams discloses a method wherein the at least one queue includes a first instruction queue associated with the processor (Column 4, lines 18-22).

10. For Claim 23, Williams discloses a method wherein the at least one queue further includes a second instruction queue associated with a second processor (Column 6 lines 8-12).

11. For Claim 24, Williams discloses a method wherein the prediction of load of the system is based on the complexity of the instructions stored in the at least one queue (Column 2, lines 2-11).

12. For Claim 25, Williams discloses a method wherein the prediction of the load of the system is based on the complexity of a subset of the instructions stored in the at least one queue (Column 2, lines 2-11,25-26).

13. For Claim 26, Williams discloses a method of claim 21 wherein the prediction of the load of the system is based, at least in part, on a subset of the instructions (Column 2, lines 2-11,25-26).

14. For Claim 27, Williams discloses a method wherein the prediction of the load of the system load includes a short term load prediction and a long term load prediction (Column 2-18 [William allow the load estimation to come from the whole list of instructions/software program or a portion of it).

15. For Claim 28, Williams discloses a method wherein the short term load prediction is based on instructions likely to be executed in the short term (Column 2-18).

16. For Claim 30, Williams discloses a method wherein the long term prediction is based on instructions likely to be executed in the long term (Column 2, lines 2-18).

17. For Claim 32, Williams discloses a computer system comprising:

> (a) at least one processor; (b) at least one queue which stores instructions for execution by the processor; (c) a clock electrically coupled to the processor; and (d) a clock estimation device electrically coupled to the queue and the clock, the clock estimation device being configured to control the frequency of a clock signal output from the clock to the processor (Figure 2, Column 2, lines 39-45).

18. For Claim 33, Williams discloses a computer system wherein initially the processor runs at an initialization clock frequency, and subsequent clock frequencies are determined by the clock estimation device based on the number instructions stored in the queue (Column 6, lines 33-42).

19. For Claim 34, Williams discloses a computer system of claim 33 wherein the subsequent clock frequencies are selected from a plurality of available clock frequencies (Column 2, lines 38-39).

20. For Claim 35, Williams discloses a computer system wherein the processor is a microprocessor (Figure 3).

21. For Claim 35, Williams discloses a computer system wherein the processor is a central processing unit (CPU) (Figure 2).

22. For Claim 38, Williams discloses a computer system further comprising: (e) a temperature monitor device electrically coupled to the processor and the clock estimation device for maintaining the computer system at an acceptable range of operating temperature, wherein the clock estimation device factors in a temperature measured by the temperature monitor device (Column 5, lines 41-45).

23. For Claim 40, Williams disclose a computer system comprising: (a) a first processor; (b) a first load and clock estimation device electrically coupled to the first processor; (c) a second processor; (d) a second load and clock estimation device electrically coupled to the second processor; and (e) an instruction cache electrically coupled to the first and second processors and at least one of the first and second load and clock estimation devices, wherein the first and second load and clock estimation devices are synchronized (Column 5, lines 64-67, Column 6, lines 1-15) .

24. For Claim 41, Williams discloses a computer system further comprising: (f) a first clock electrically coupled to the first processor and the first load and clock estimation device; and (g) a second clock electrically coupled to the second processor and the second load and clock estimation device, wherein the first load and clock estimation device is configured to control the frequency of a first clock signal output from the first clock to the first processor, and the second load and clock estimation device is configured to control the frequency of a second clock signal output from the first clock to the first processor (Column 5, lines 64-67, Column 6, lines 1-15).

25. Claim 45 rejected under 35 U.S.C. 102(b) as being anticipated by McDermott (US 5,815,693).

26. For Claim 45, McDermott discloses a computer system comprising: (a) an optimum clock estimation device; (b) at least one long term load estimation device electrically coupled to the optimum clock estimation device (Figure 3, [301b]); (c) at least one short term estimation device electrically coupled to the optimum clock estimation device (Figure 3 [301b]); (d) a clock electrically coupled to the optimum clock estimation device (Figure 3); and (e) a processor electrically coupled to the clock, wherein each of the long term and short term load estimation devices analyze a set of instructions, and the optimum clock estimation device controls the frequency of a clock signal output from the clock to the processor based on at least one of the long term and short term analysis (Figures 2a and 3, Column 8, lines 29-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 13-14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claims 11 and 12 above, and further in view of Sheets (US 4,670,837).

28. For Claim 13, Sheets discloses a method wherein the at least one instruction has a predetermined weight, the predetermined weight varying according to the type of the at least one instruction(Column 3, lines 25-28).

29. For Claim 14, Sheets discloses a method the estimation of step (b) changes based, at least in part, upon the predetermined weight (Column 3, lines 46-52).

30. For Claim 16, Sheets discloses a method wherein the at least one instruction is generated automatically (Column 3, lines 34-37).

31. Williams, however does not teach of applying a predetermined weight to an instruction based on its type. Specifically, Williams teaches of the calculation of the load being determined by the complexity of the program/part of the program/instruction. It would have been obvious to one of ordinary skill in the art to combine the teachings of Williams and Sheets because they both deal with methods for reducing power consumption by adjusting the clock frequency of the processor and the dependant on the complexity of the load/instructions. Sheets teaches the method of applying a predetermined weight to an instruction based on its type and using this in the estimation of load of the system. This provides means to be more accurate in the load estimation and can allow the system to choose a clock frequency that increases the optimization and further reduces power consumption.

Allowable Subject Matter

32. Claims 29, 31, 36-37, 39 42-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

33. Claims 11-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,715,089 B2. Although the conflicting claims are not identical, they are not patentably distinct from

each other because the input is declared to be an instruction throughout the claims and all the instructions are connected to the queue.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin L. Dogan whose telephone number is 571-272-1412. The examiner can normally be reached on Mon-Fri 8:00-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin Dogan
Patent Examiner
Art Unit 2115

CHUN CAO
PRIMARY EXAMINER